IN THE CLAIMS:

Please cancel claims 28-32.

Please amend claims 21, 24, 27, 33, 36, 37, 40, 41, and 44.

21. (Amended) A semiconductor device comprising:

a gate member on a semiconductor;

a source region in the semiconductor;

[source and] a drain region in the semiconductor, [one of] said [source and] drain region[s] having a depth shallower than said source region and not deeper than 0.1 μm;

a channel region being interposed between said source and drain regions and being adjacent to said gate electrode, said channel region having a length not longer than 1μm, and

wherein said source and drain regions extends from a surface of said semiconductor to said depth not longer than a thickness of said semiconductor,

wherein said source region overlaps with said gate member while said drain region has an edge which coincides with that of said gate member.

24. (Amended) A memory comprising:

a gate electrode having a floating gate, a control gate and an oxide on a semiconductor substrate, said oxide being provided on surfaces of the floating gate and the control gate;

a source region in the semiconductor;

[source and] a drain region in the semiconductor, [one of] said

[source and] drain region[s] having a depth shallower than said source region and not deeper than 0.1 μm; and

a channel region being interposed between said source and drain regions being adjacent to said gate electrode, said channel region having a length not longer than 1μm,

wherein an edge of said [one of the source and] drain region[s] [is] coincides with that of said gate electrode, and

wherein [the other one of] said source [and drain] region[s] overlaps with said gate electrode.

7 ~~27.~~ (Amended) A semiconductor device according to claim ~~24~~ wherein said floating gate is formed [on] over [the other one of] said source [and drain] region[s] while said floating gate is not formed [on] over said [one of the source and] drain region[s].

8 ~~33.~~ (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first silicon film introduced with an n-type impurity over said semiconductor substrate;

a second silicon film introduced with an n-type impurity over said first silicon film;

an insulating film interposed between said semiconductor substrate and said first silicon film and between said first and second silicon film;

a first impurity region formed in the semiconductor substrate, said first impurity region overlapping with said insulating film;

a second impurity region formed in the semiconductor substrate, said second impurity region having an edge which coincides with that of said insulating film, being not contact with said first impurity region [an] , and having a depth shallower than said first impurity region and not deeper than 0.1 μm;

a channel region formed between said first and second impurity region, said channel region having a length not longer than 1 μm.

36. (Amended) A semiconductor device according to claim 33 wherein a floating gate is formed [on] over said first impurity region while said floating gate is not formed [on] over said second impurity region.

~~37.~~ 12 (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least two gate electrodes over said semiconductor substrate;

a first impurity region formed between said gate electrodes;

at least two second impurity regions formed [in] adjacent [with] to said gate electrodes, each of said second impurity region having a depth shallower than that of said first impurity region; and

at least two channel regions in the semiconductor substrate, each of said channel regions being formed between said first impurity region and each of second impurity regions, and being adjacent to each of said gate electrodes,

wherein each of said channel regions has a length not longer than 1 μm,

wherein said depth of each of said second impurity regions is not

deeper than 0.1 μm, and

wherein said first impurity region overlaps with each of said gate electrodes while each of said second impurity regions has an edge which coincides with that of each of said gate electrodes.

15 ~~40.~~ (Amended) A semiconductor device according to claim 12 ~~37~~ wherein a floating gate is formed [on] over said first impurity region while said floating gate is not formed [on] over each of said second impurity regions.

16 ~~41.~~ (Amended) A semiconductor device comprising:

a semiconductor substrate;

at least two gate electrodes over said semiconductor substrate, each of said gate electrodes having a floating gate, a control gate and an oxide on said semiconductor substrate, said oxide being provided on surfaces of the floating gate and the control gate;

a first impurity region formed between said gate electrodes;

at least two second impurity regions formed in adjacent with said gate electrodes, each of said second impurity region having a depth shallower than that of said first impurity region; and

at least two channel regions in the semiconductor substrate, each of said channel regions being formed between said first impurity region and each of second impurity regions,

wherein each of said channel regions has a length not longer than 1 μm,

wherein said depth of each of said second impurity regions is not